

(19)



JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: 05136323 A

(43) Date of publication of application: 01.06.93

(51) Int. Cl.

H01L 23/50

(21) Application number: 03297304

(22) Date of filing: 13.11.91

(71) Applicant: NEC CORP NEC ENG LTD

(72) Inventor: YOSHINO SUSUMU
CHIKAMA HIROKI

(54) INTEGRATED CIRCUIT DEVICE

(57) Abstract:

PURPOSE: To relax the limits to the integration density and to the number of signal pins of a single LSI chip when the LSI chip is mounted on an integrated circuit package and to relax the influence of a noise caused at the LSI chip and at leads.

CONSTITUTION: A plurality of LSI chips 5 are mounted at the upper part and the lower part so as to sandwich a support plate 9 or a support plate 9 which can be grounded. In such an integrated circuit structure, the LSI chips at the upper part and the lower part are connected to leads or a lead frame 1 by means of bonding wires 2. When the two chips at the upper part and the lower part are die-bonded, they are connected to the leads or the lead frame 1. The leads have a structure which is divided into the upper part and the lower part or into the right and the left so as to sandwich the support plate 9 which can be grounded; they are connected to the individual chips. Thereby, the chips can be integrated highly and mounted at high density, and their noise can be reduced.

COPYRIGHT: (C)1993,JPO&Japio

